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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/600,048
Filing Date: June 19, 2003
Appellant(s): LIPPINCOTT, LOUIS A.

LIPPINCOTT, LOUIS A.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/4/2009 appealing from the Office action mailed 4/17/2008

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,933,836	Tulpule et al.	06-1990
6,967,950	Galicki et al.	11-2005
6,757,019	Hsieh et al	06-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 10, 12, 18, 19, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836, Tulpule, hereinafter) in view of Galicki et al. (U.S. Patent No. 6,967,950, hereinafter, Galicki).

As per claim 1, Tulpule teach an apparatus comprising:

a first processor 12 (Fig. 1) *having two or more processor elements* (Fig. 7, col. 13, ll. 32-48), *and two or more input/output ports coupled together by a first port ring this is within the first processor* (Fig. 2, col. 8, ll. 34-40); and

a second processor 18, which is similar to the first processor 12 (see also Fig. 7), *couples to the first processor* 12 *through at least one I/O port of a third port ring within a third processor* 14 (Fig. 1).

Tulpule fails to teach *the two or more I/O ports in the first processor, the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor, the logical connection to originate at first processor and to traverse through the third processor and to complete at the second processor, wherein the logical connection is established based on other active logical connections that include at least*

one of the first processor, the second processor and third processor. However, this is what Galicki teaches. As shown in Fig. 2, Galicki teach an array of multiple processors that are configured to establish a logical connection between the first processor (e.g. DSP #1) and the second processor (e.g. DSP #7) (col. 4, lines 21-44), wherein the logical originate at the first processor DSP #1 and to traverse through the third processor (e.g. DSP # 2) and to complete at the second processor DSP #7, *wherein the logical connection is established based on other active logical connections that include at least one of the first processor, the second processor, and the third processor* (i.e. based on other active receive channels as shown in Figs. 7-9, see col. 8, lines 48-56, …there can be only one active channel at any one time, so a packet that wants to deposit its data into a specific channel, should contain a CHAN rx_opcode in its header to activate the correct channel before the body of the packet reaches the receiver. If the first, second, or third processor is not the active received channels, data can exit the DSP through the left or right port, see Fig. 6, col. 6, lines 43-55, i.e. depending on other logical connections). (It is also noted that Galicki teaches *broadcast packets can navigate to multiple destinations* (col. 5, lines 48-62); that means more than one logical connections are established between the processors).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Galicki in combination with the method as taught by Tulpule in order to increase system performance, simplifying software and decreasing central processing unit/direct memory access loading (col. 10, lines 55-67).

As per claim 2, as shown in Fig. 1, Tulpule, teach the two or more I/O ports of the first processor is not directly connected to the two or more I/O ports of the second processor.

As per claims 3, Tulpule fails to teach the first, second, and third processors are part of a number of processors in a point-to-point configuration. However, Galicki et al. teach a method of transferring data between multiple digital signal processors from the source processor 201 to the destination processor in a point-to-point configuration (Fig. 2, col. 4, ll. 45-55).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Galicki in combination with the method as taught by Tulpule in order to increase system performance, simplifies software and decreases central processing unit and direct memory access unit loading (col. 3, ll. 10-20).

As per claim 4, although Tulpule does not explicitly teach the first processor transmitting output from an image process operation to the second processor, Tulpule does teach the processors are the signal processors, and also suggest using for image processing (col. 1, ll. 61-68). Although Tulpule fails to teach transmitting of image data to the second processor from the first processor based on a logical connection, Galicki teaches this feature as cited above (implemented via the datapipe).

As per claim 5, although Tulpule fails to explicitly teach the I/O ports of the processors comprising a FIFO memory, Tulpule does teach at the I/O ports of the signal processor 12 (such as "North" and "South" ports, Fig. 3) comprising a dual port RAM 74 and 76 to communicate with other modular entities (col. 10, ll. 36-41). Therefore, it would have been obvious to one skilled in the art to modify the memories 74 and 76 into FIFO in order to queue the commands received or transmitted at each processor.

As per claim 6, Tulpule does not explicitly teach the I/O ports of each processor comprising a transmitter port and receiver port, wherein the first processor configured to transmit

the output based a handshake protocol among the receiver ports and the transmitter ports of the first processor, the second processor, and the third processor. However, this is taught by Galicki with reference to Figs. 10 and 11.

As per claim 7, as cited above, the teachings of Tulpule and Galicki in combination teach the limitations of claim 7. Specifically, Tulpule teach a plurality of signal processors 12-18, each includes plurality of I/O ports configured in a port ring, at least one signal processor 24, which may be used in image processing, wherein one signal processor coupled to another signal processor via the I/O ports of the port rings. Galicki teach the digital signal processors are coupled together in a point-to-point configuration. With reference to claim 1, Galick teach the number of ports within the port rings of the number of image signal processors are configured to establish logical connections between the number of image signal processors, wherein the logical connections are to originate at a source image signal processor (DSP#1) of the number of image signal processors and to traverse a number of intermediate image signal processors (DSP#2, DSP#3) of the number of image signal processors and to complete at a destination image signal processor (DSP#7) of the number of image signal processors, wherein the source image signal processor is to transmit an initialize signal (included in the packet header, col. 7, lines 30-35, and col. 6, lines 43-55), prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection (col. 5, lines 49-61, and col. 8, lines 48-56).

As per claim 8, as cited above, the combined system teaches the at least one processor element in a first of the number of image processors is configured to perform one of a number of image processed-based operations.

Claims 10 and 12, which are similar to claims 4 and 5, are thus rejected under the same rationale.

As per claim 18, the limitations of which have been addressed above with reference to claims 1 and 7, further requires registering a logical connection with a number of ports of port rings of a number of image signal processors in a logical connection based on transmission of an initialization signal through a logical connection. However, this is also taught by Galicki as cited above, wherein the header packet is examined at the I/O port of each DSP (col. 6, lines 43-55).

Claims 19, 21-24, which are similar in scope to claims 6-10, 12, and 18 above, are rejected under similar rationale.

3. Claims 13-15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836) in view of Galicki et al. (U.S. Patent No. 6,967,950), and further in view of Hsieh et al. (U.S. Patent No. 6,757,019, hereinafter, Hsieh).

As per claim 13, the teachings of Tulpule and Galicki are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach or suggest a CMOS sensor to capture image data. This is what Hsieh teaches. As shown in Figs. 3 and 4, Hsieh teaches an image processor including a plurality of image signals processors 40, having a plurality of expansion interfaces (DMA 50, Fig. 5) configured to receive the image data to captured by the CMOS sensor 22 (col. 5, ll. 1-14). Hsieh also teaches the host processor

configure a number of logical connection among the number of image signal processors 40 (Figs. 2A-2C, col. 4, ll. 13-24).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Hseih in combination with the method as taught by Tulpule and Galicki because CMOS image sensor provides high speed video capturing and thus further increase the overall image processing performance. Therefore, at least claim 13 would have been obvious.

As per claim 14, the combined system provides at least one image signal processor comprises a hardware accelerator (such as signal processor, Tulpule, or PEs 40, of Hsieh) to execute image process operations.

As per claim 15, Hsieh teaches the image processor comprises a global bus (such as, bus connects the PEs as shown in Fig. 2C) coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

As per claim 17, Galicki teaches traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processors (Fig. 2, col. 4 12, ll. 45-55).

(10) Response to Argument

Appellant's arguments filed 1/7/2008 have been fully considered but they are not persuasive. In response to Appellant's arguments that the cited reference do not disclose *a logical connection is established based on other active logical connections among the processors,* this limitation is addressed in details above in the rejections of the claim 1, that is, based on other

active receive channels as shown in Figs. 7-9, see col. 8, lines 48-56, where Galicki, the secondary reference teaches:

> …During typical operation, data packets arriving to the receiver from the center port of the local bridge are packed into words and transferred to the local I/O RAM at the current address of the active receive channel. There can be only one active channel at any one time, so a packet that wants to deposit its data into a specific channel, should contain a CHAN rx_opcode in its header to activate the correct channel before the body of the packet reaches the receiver".

If the first, second, or third processor is not the active received channels, data can exit the DSP through the left or right port, (see Fig. 6, col. 6, lines 43-55, i.e. depending on other logical connections). It is also noted that Galicki teaches *broadcast packets can navigate to multiple destinations* (col. 5, lines 48-62); that means more than one logical connections are established between the processors.

In regard to Appellant's arguments that the cited references do not teach *where the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processor to the destination image signal processor in the order that data is transmitted in the logical connections,"* the examiner also disagrees. In fact, on col. 5, lines 49-61, Galicki teaches:

> *A typical transfer starts at the source digital signal processor where a packet is injected into the datapipe network through one of the transmit channels. The header preceding the packet content contains information about one or more destinations for the packet.* As the packet enters each node, the header is examined with reference to the local identification code (ID) registers inside the datapipe bridge. The bridge left and bridge right ID registers have knowledge of the location of all other processors within a communications cell of up to 32 processors. The packet may be accepted into the node, routed back out through the left or right port, whichever is closer to the destination encoded in the header, or both accepted into the node and routed to the port.

and further teaches:

… a packet that wants to deposit its data into a specific channel, should contain a CHAN rx_ opcode in its header to activate the correct channel *before the body of the packet reaches the receiver.* (col. 8, lines 48-56, emphasis added).

Thus, the headers is initialized and transmitted to the destination processor. The header is then evaluated first at the destination processor prior to accepting the data.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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